[0171] The data input/output circuit **217** may be connected to the sense amplifier and write driver circuit **215** through the data lines DL. The data input/output circuit **217** may output data, which is read by the sense amplifier and write driver circuit **215**, to the controller through an input/output channel and may transfer data, which is received from the controller through the input/output channel, to the sense amplifier and write driver circuit **215**.

[0172] The control logic circuit **219** may receive a command from the controller through the input/output channel and may receive a control signal therefrom through a control channel. The control logic circuit **219** may receive a command through the input/output channel in response to the control signal, may route an address, which is received through the input/output channel, to the row decoder circuit **213**, and may route data, which is received through the input/output channel, to the data input/output circuit **217**. The control logic circuit **219** may decode the received command and may control the nonvolatile memory device **210** based on the decoded command.

[0173] FIG. **14** is a circuit diagram illustrating a memory tile TILEk according to example embodiments of inventive concepts. As illustrated in FIG. **14**, a memory tile TILEk may include word lines and bit lines sequentially stacked along a height direction. For example, in FIG. **14**, bit lines BL**1**_**1** and BL**1**_**2** may be disposed at a first plane. The bit lines BL**1**_**1** and BL**1**_**2** may extend along a column direction and may be spaced from each other along a row direction.

[0174] Word lines WL**1**_**1** and WL**1**_**2** may be disposed at the second plane on the second plane. The word lines WL**1**_**1** and WL**1**_**2** may extend along a row direction and may be spaced from each other along a column direction.

[0175] Memory cells may be formed between the first plane and the second plane and may be respectively disposed at cross-points of the bit lines BL**1**_**1** and BL**1**_**2** and the word lines WL**1**_**1** and WL**1**_**2**. Each memory cell may be connected to a word line and a bit line.

[0176] Bit lines BL**2**_**1** and BL**2**_**2** may be disposed at a third plane on the second plane. The bit lines BL**2**_**1** and BL**2**_**2** may extend along the column direction and may be spaced from each other along the row direction.

[0177] Memory cells may be formed between the second plane and the third plane and may be respectively disposed at cross-points of the bit lines BL**2**_**1** and BL**2**_**2** and the word lines WL**1**_**1** and WL**1**_**2**. Each memory cell may be connected to a word line and a bit line.

[0178] Word lines WL**2**_**1** and WL**2**_**2** may be disposed at a fourth plane on the third plane. The word lines WL**2**_**1** and WL**2**_**2** may extend along the row direction and may be spaced from each other along the column direction.

[0179] Memory cells may be formed between the third plane and the fourth plane and may be respectively disposed at cross-points of the bit lines BL**2**_**1** and BL**2**_**2** and the word lines WL**2**_**1** and WL**2**_**2**. Each memory cell may be connected to a word line and a bit line.

[0180] Each memory cell may include a variable resistor element VR and a selection element S. A resistance value of the variable resistor element VR may increase (e.g., may be set or written) when voltages of a word line and a bit line belong to a first condition. A resistance value of the variable resistor element VR may decrease (e.g., may be reset or erased) when voltages of a word line and a bit line belong to a second condition. A resistance value of the variable resistor element VR may be maintained when word line and bit line voltages do not belong to the first and second conditions.

[0181] The selection element S may include a diode. The selection element S may provide selectivity of a corresponding memory cell. For example, the selection element S may select a corresponding memory cell by passing a current based on voltages of a word line and a bit line. The selection element S may not select a corresponding memory cell by blocking a current based on voltages of a word line and a bit line. In example embodiments, the selection element S may be replaced with a transistor. In example embodiments, a method of controlling voltages of a word line and a bit line may be used to select each memory cell, instead of using the selection element S. For example, no current may flow to an unselected memory cell by setting a word line and a bit line, which are connected to the unselected memory cell, with the same voltage. A current may flow to an unselected memory cell by setting a word line and a bit line, which are connected to the unselected memory cell, with different voltages. In the case where the method of adjusting voltages is used instead of the selection element S, each memory cell may not include the selection element S.

[0182] The variable resistor element VR may be of a resistive type, a phase-change type, a magnetic type, or a ferroelectric type.

[0183] As described above, the memory tiles TILE**1** to TILEz may share the global bit lines GBL. Each global bit line may be connected with a plurality of bit lines in each memory tile. Due to a resistive load and a capacitive load of each global bit line, thus, a lot of time may be taken to drive each global bit line up to a target voltage. The driver circuit **13**, **14**, **15**, or **16** according to example embodiments of inventive concepts may be used to reduce a time taken to drive each global bit line up to a target voltage. Likewise, the driver circuit **13**, **14**, **15**, or **16** according to example embodiments of inventive concepts may be used to reduce a time taken to drive each global word line up to a target voltage.

[0184] FIG. **15** is a block diagram partially illustrating a row decoder circuit **213_1** and a sense amplifier and write driver circuit **215_1** to each of which a driver circuit according to example embodiments of inventive concepts is applied.

[0185] Referring to FIG. **15**, a row decoder circuit **213_1** may include a global word line driver corresponding to a global word line GWL. The global word line driver may be configured to drive a global word line using one or more of the driver circuits **13** to **16** described with reference to FIGS. **5** to **8**.

[0186] A sense amplifier and write driver circuit **215_1** may include a global bit line driver which drives a global bit line. The global bit line driver **215_1** may be configured to drive a global bit line GBL using one or more of the driver circuits **13** to **16** described with reference to FIGS. **5** to **8**.

[0187] FIG. **16** is a block diagram illustrating a storage device **100** according to example embodiments of inventive concepts. Referring to FIG. **16**, a storage device **100** may include a nonvolatile memory device **110**, a controller **120**, and a random access memory (RAM) **130**.

[0188] The nonvolatile memory device **110** may perform a write, read or erase operation under control of the controller **120**. The nonvolatile memory device **110** may receive a command and an address from the controller **120** through